

# FIG. 1

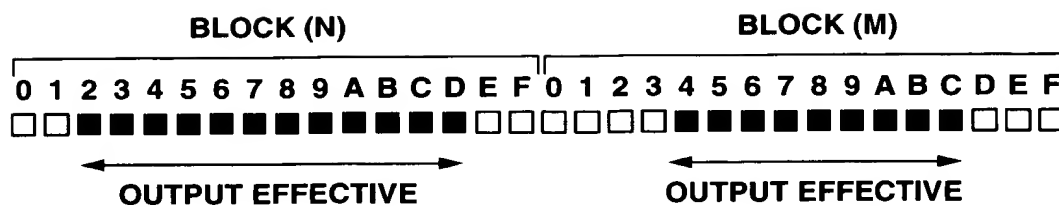


FIG.2

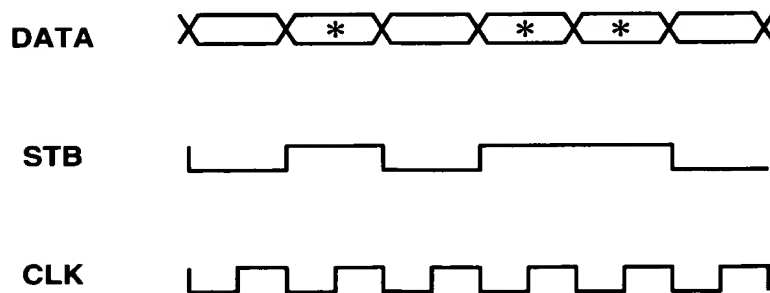


FIG.3

PB\_DATA

FIG.4A

BUFF\_WR

FIG.4B

ECC

FIG.4C

BUFF\_RD

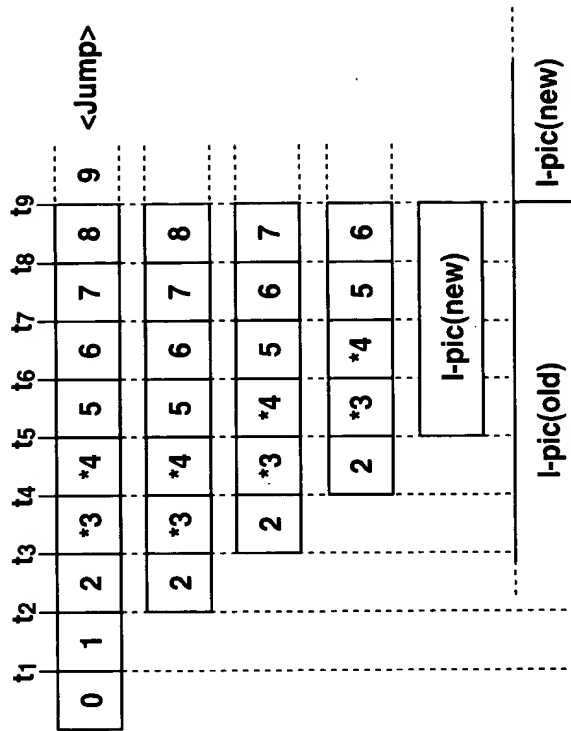
FIG.4D

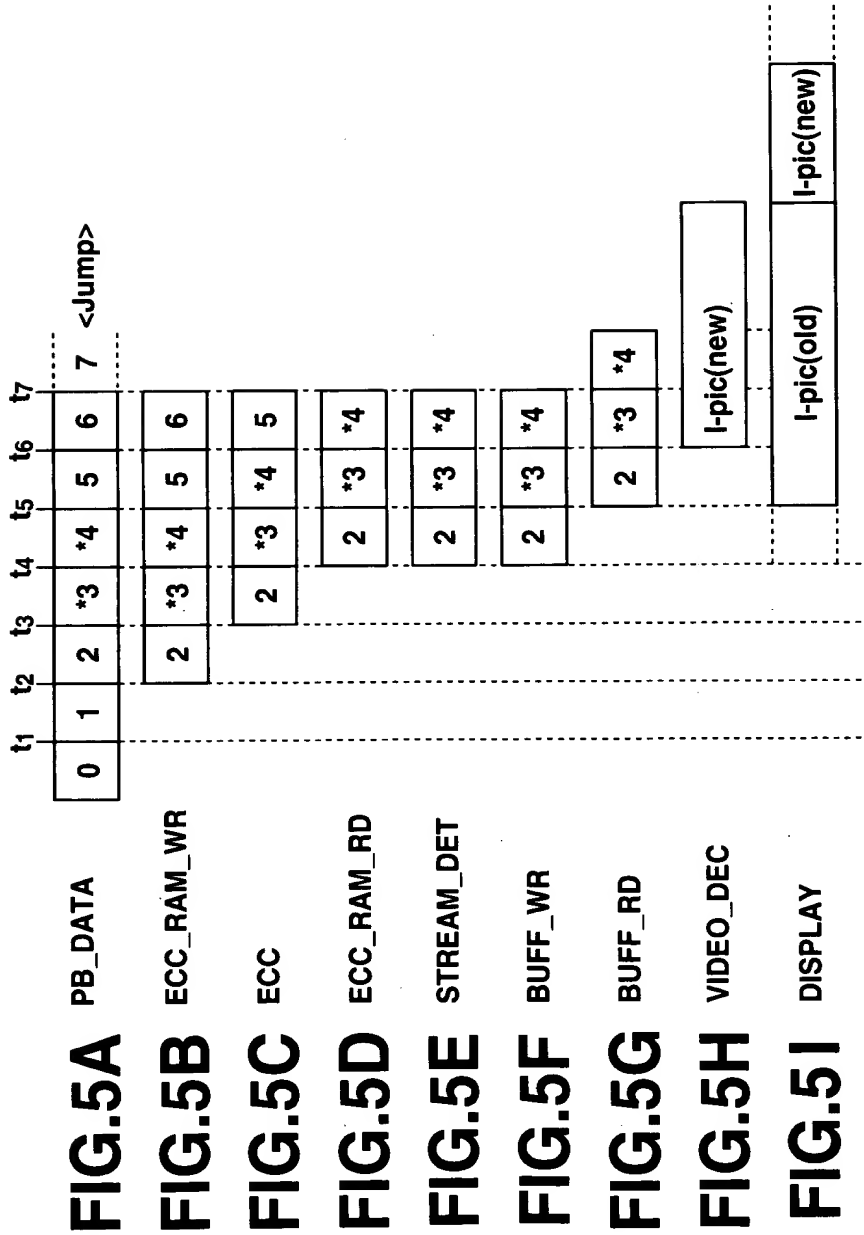
VIDEO\_DEC

FIG.4E

DISPLAY

FIG.4F





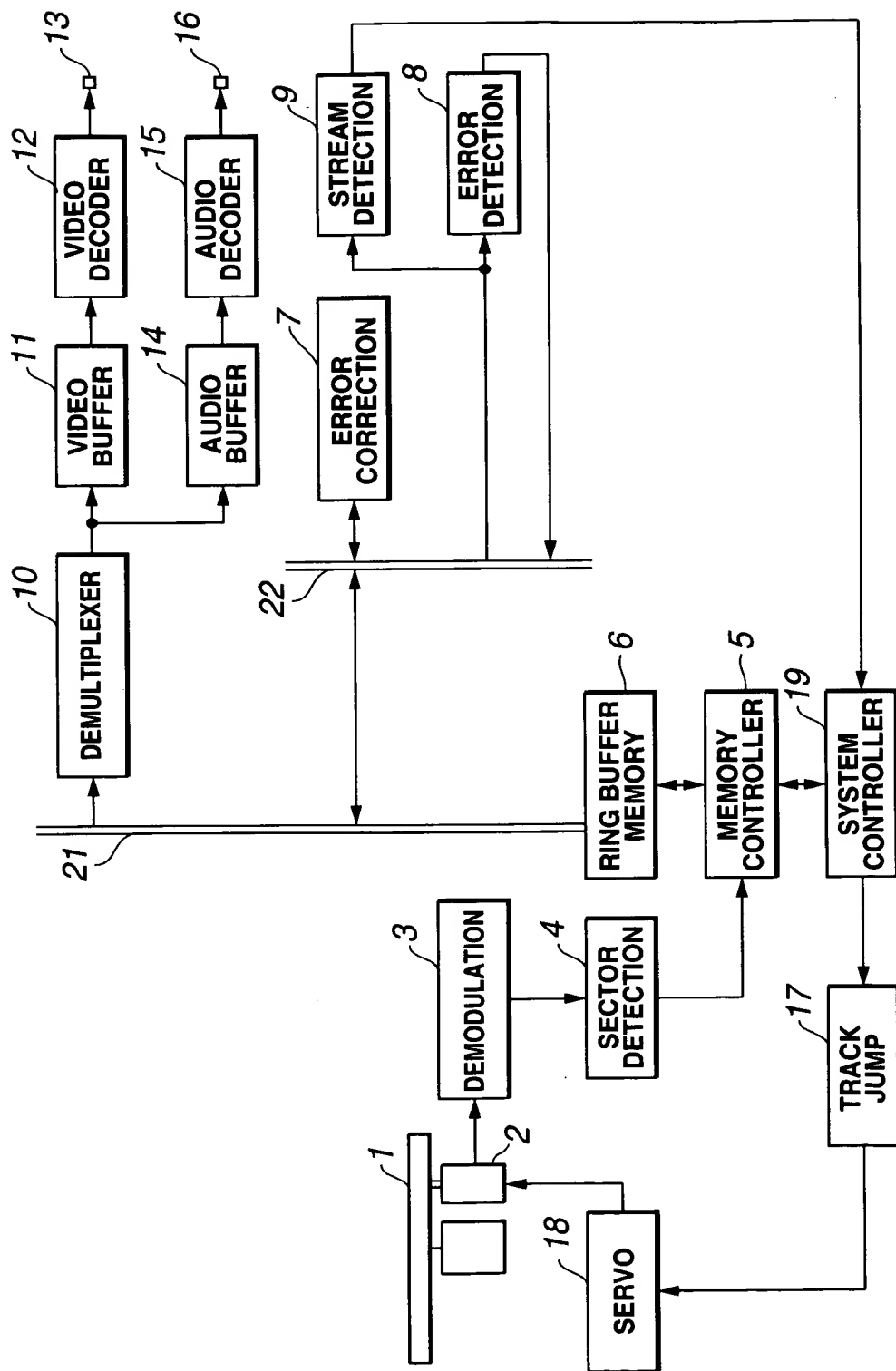


FIG. 6

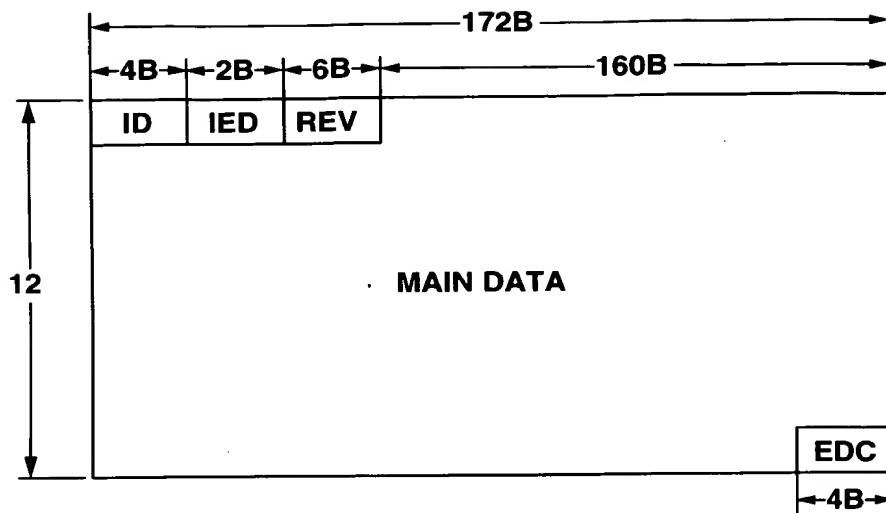


FIG. 7

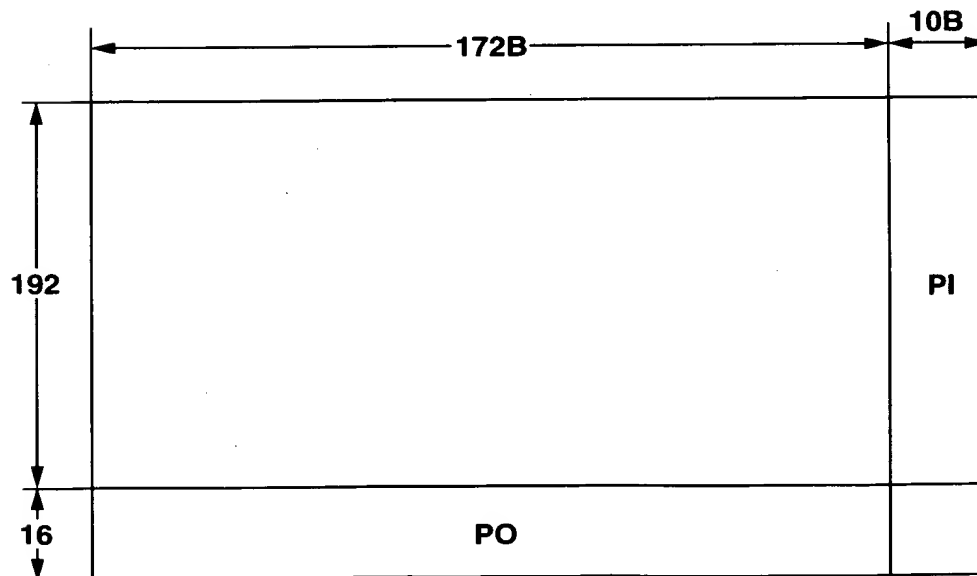
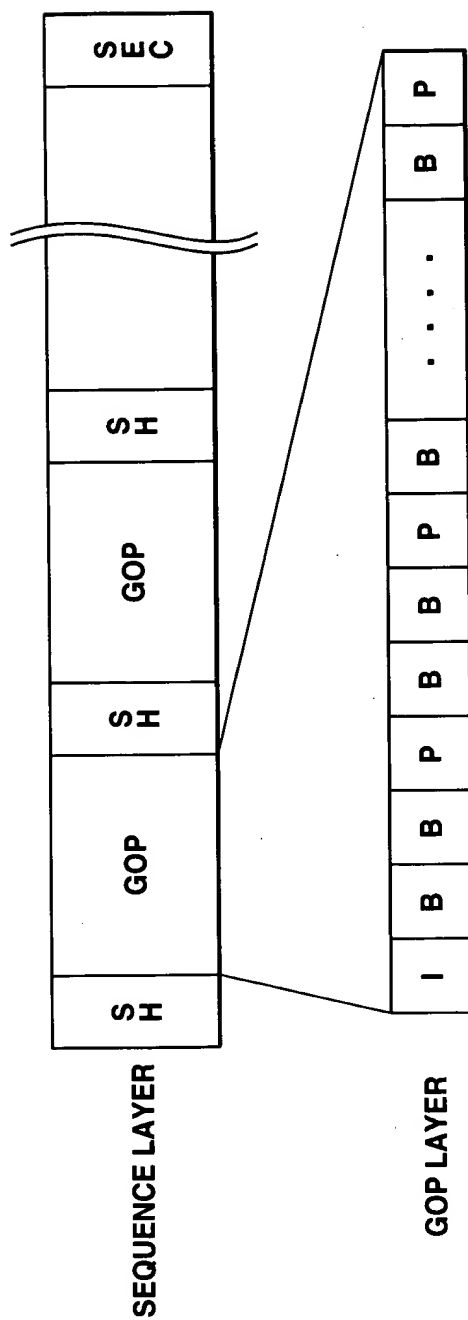


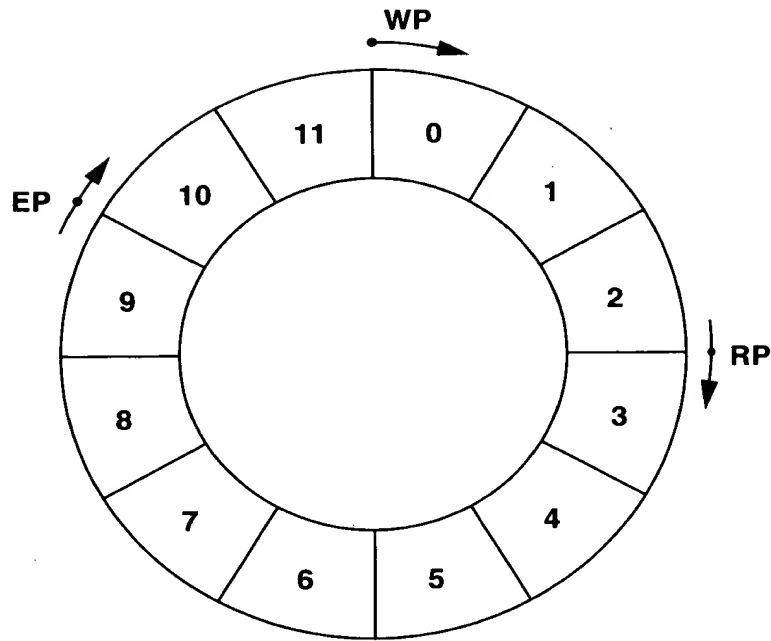
FIG. 8

32BITS		1456BITS		32BITS		1458BITS	
SY0	ID IED			SY5		P1	
SY1				SY5		P1	
SY2				SY5		P1	
SY3				SY5		P1	
SY4				SY5		P1	
SY1				SY6		P1	
SY2				SY6		P1	
SY3				SY6		P1	
SY4				SY6		P1	
SY1				SY7		P1	
SY2				SY7		P1	
SY3				SY7		EDC P1	
SY4	P0			SY7		P0	P1

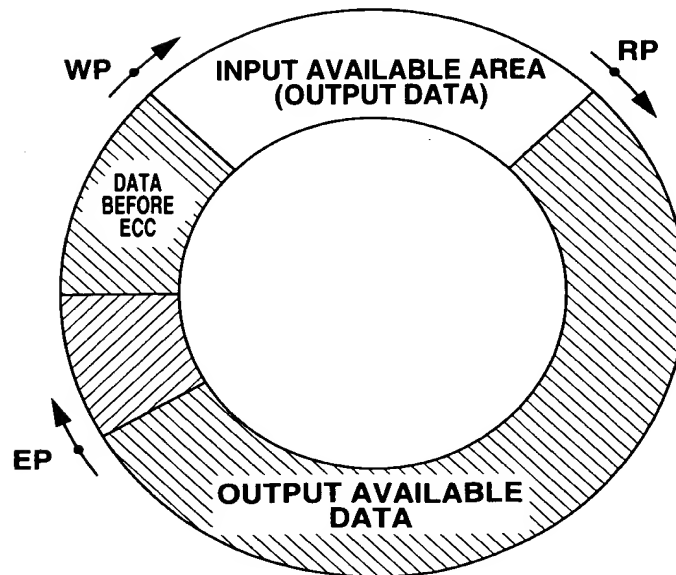
FIG.9



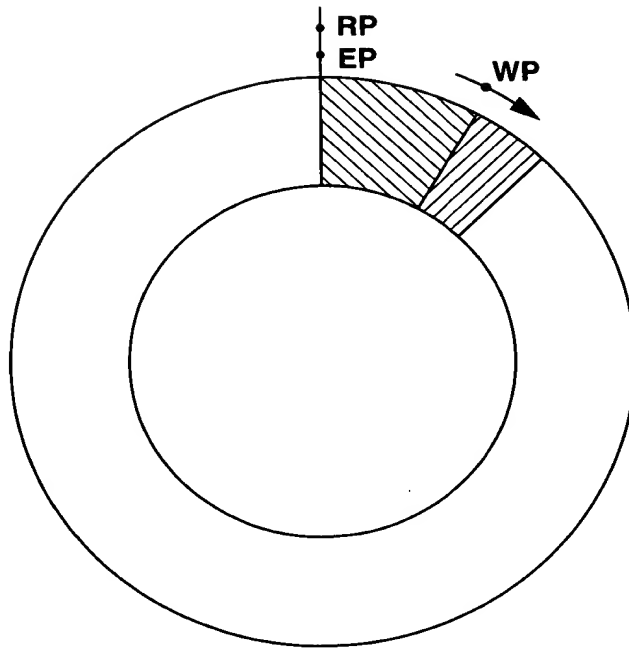




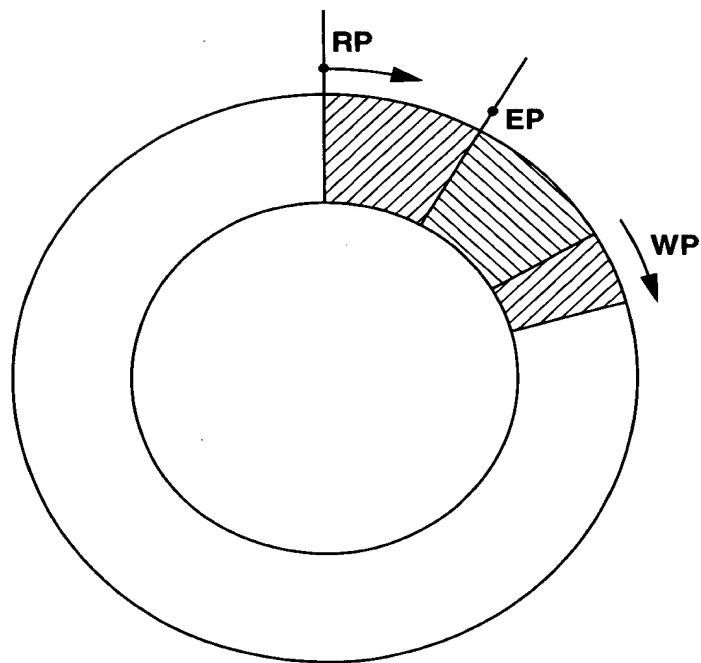
**FIG.11**



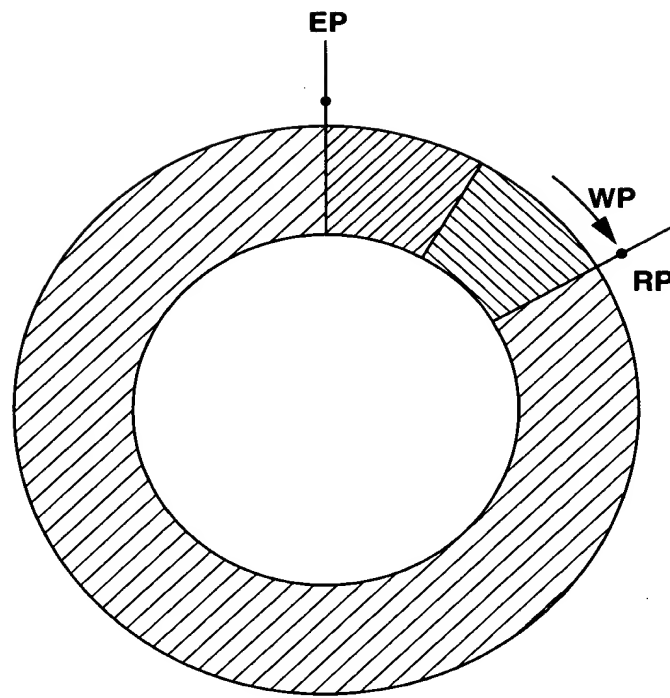
**FIG.12**



**FIG.13**



**FIG.14**



**FIG.15**

**FIG.16**

FIG.17A

PB\_DATA

t1	t2	t3	t4	t5	t6
0	1	2	*3	*4	5
					6
					<Jump>

FIG.17B

BUFF\_WR

2	*3	*4	5
			<WR_STOP>

FIG.17C

ECC(+STREAM\_DET)

2	*3	*4
		<ECC_STOP>

FIG.17D

IP\_END\_DET

IP\_END\_DET

2	*3	*4
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FIG.17E

VIDEO\_DEC

I-pic(new)
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FIG.17F

DISPLAY

I-pic(old)	I-pic(new)
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